METHOD AND APPARATUS FOR DYNAMIC REGISTER MANAGEMENT IN A PROCESSOR

ABSTRACT

A method for mapping a plurality of virtual registers to a plurality of physical registers is provided. Generally, a plurality of virtual registers are provided where each virtual register comprises physical register address bits. A status indicator for indicating the status of each virtual register is also provided.

A processing device is also provided. The processing device has a plurality of physical registers. A plurality of virtual registers, wherein each virtual register comprises physical register address bits form part of the processing device. The processing device also has a status indicator for indicating a status of each virtual register.